Notice of Allowability	Application No.	Applicant(s)	
	09/775,950	CHEN ET AL.	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the appeal brief filed on 09/27/04*.

2. ☒ The allowed claim(s) is/are *1-19*.

3. ☒ The drawings filed on *02 February 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY J. LAMARRE
PRIMARY EXAMINER

DETAILED ACTION

Response to the applicant's amendments

******** The amended claim (claim 1) to overcome 101 rejections is accepted by the examiner.

Examiner's statement for reason for allowance

The following is an examiner's statement for allowance:

1. Claims **1-19** have been allowed.

As per claim **1,** the prior art, (Eroz et al. U.S. PN: 6,333,197) teach or disclose interleavers implemented by the interleaver (see fig. 2, element 16) is a two-dimensional block interleaver (or interleaver matrix) is a number rows and a number of columns whereby an input data are written into the interleaver matrix row by row and then row and column permutations are performed to randomize data positions wherein the data are then read out column by column (see col. 9, lines 2-10). Further, Eroz et al. teach an input position, a corresponding output interleaved position given by mathematical formula, wherein a column permutation applied to data in a row and to a bit-reversed indexing, which is especially simple to implement and requires no additional parameter storage in the memory of the interleaver (16) (see col. 9, lines 11-17). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious bit reversing row indexes for a first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for a second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns. Consequently, claim 1 is allowed over the prior art.

Claims **2-6,** which are directly or indirectly dependents of claim 1 are also allowable over the prior art of record.

As per claim 7, the prior art, (Eroz et al. U.S. PN: 6,333,197) teach or disclose interleavers implemented by the interleaver (see fig. 2, element 16) is a two-dimensional block interleaver (or interleaver matrix) is a number rows and a number of columns whereby an input data are written into the interleaver matrix row by row and then row and column permutations are performed to randomize data positions wherein the data are then read out column by column (see col. 9, lines 2-10). Further, Eroz et al. teach an input position, a corresponding output interleaved position given by mathematical formula, wherein a column permutation applied to data in a row and to a bit-reversed indexing, which is especially simple to implement and requires no additional parameter storage in the memory of the interleaver (16) (see col. 9, lines 11-17). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a controller configured to bit reversing row indexes for a first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for a second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns and an output device configured to sequentially read the interleaved input memory addressed from the columns of the matrix and read and transmit data elements stored at corresponding memory addresses in the sequential read order of the interleaved input memory addresses. Consequently, claim 7 is allowed over the prior art.

Claims **8-12,** which are directly or indirectly dependents of claim 7 are also allowable over the prior art of record.

As per claim **13,** the prior art, (Eroz et al. U.S. PN: 6,333,197) teach or disclose interleavers implemented by the interleaver (see fig. 2, element 16) is a two-dimensional block interleaver (or interleaver matrix) is a number rows and a number of columns whereby an input data are written into the interleaver matrix row by row and then row and column permutations are performed to randomize data positions wherein the data are then read out column by column (see col. 9, lines 2-10). Further, Eroz et al. teach an input position, a corresponding output interleaved position given by mathematical formula, wherein a column permutation applied to data in a row and to a bit-reversed indexing, which is especially simple to implement and requires no additional parameter storage in the memory of the interleaver (16) (see col. 9, lines 11-17). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a controller configured to bit reversing row indexes for a first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for a second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns. Consequently, claim 13 is allowed over the prior art.

As per claim **14,** the prior art, (Eroz et al. U.S. PN: 6,333,197) teach or disclose interleavers implemented by the interleaver (see fig. 2, element 16) is a two-dimensional block interleaver (or interleaver matrix) is a number rows and a number of columns whereby an input data are written into the interleaver matrix row by row and then row and column permutations are performed to randomize data positions wherein the data are then read out column by column (see col. 9, lines 2-10). Further, Eroz et al. teach an input position, a corresponding output

interleaved position given by mathematical formula, wherein a column permutation applied to data in a row and to a bit-reversed indexing, which is especially simple to implement and requires no additional parameter storage in the memory of the interleaver (16) (see col. 9, lines 11-17). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a controller configured to bit reversing row indexes for a first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for a second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns and an output device configured to sequentially read the interleaved input memory addressed from the columns of the matrix and read and transmit data elements stored at corresponding memory addresses in the sequential read order of the interleaved input memory addresses. Consequently, claim 14 is allowed over the prior art.

Claims **15-19,** which are directly or indirectly dependents of claim 14 are also allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

GUY J. LAMARRE
PRIMARY EXAMINER